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(72) Inventor:
Tanimoto, Susumu,
c/o NEC Corporation
Tokyo (JP)

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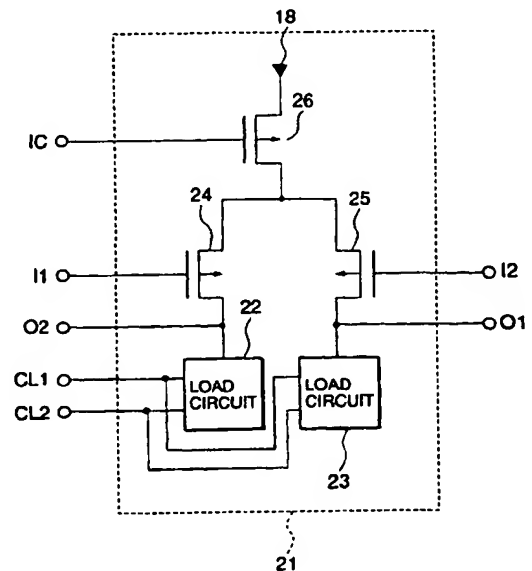
(74) Representative: **Betten & Resch**
Reichenbachstrasse 19
80469 München (DE)

(71) Applicant: **NEC CORPORATION**
Tokyo (JP)

(54) Voltage-controlled ring oscillator with differential amplifiers

(57) A voltage-controlled oscillator 3 is constructed with a ring oscillator control circuit 2 and a ring oscillator 1, which is constructed with a plurality of differential amplifiers 5 to 8 each including a differential pair of transistors 24 and 25 and load circuits 22 and 23 connected to the respective transistors. The load circuits 22 and 23 are constructed such that the differential amplifiers always operate in linear region according to load drive voltages CL1 and CL2.

Fig.4



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Description

BACKGROUND OF THE INVENTION

5 1. Field of the Invention

[0001] The present invention relates to a voltage-controlled oscillator and, particularly, to a voltage-controlled oscillator having a ring oscillator, which is constituted with a plurality of differential amplifiers each having a load circuit.

10 2. Description of the Related Art

[0002] In a recent phase-locked loop (PLL) for a disk servo system of CD-ROM, etc., an output frequency range thereof, which is up to several to ten times a reference oscillation frequency of the PLL, is required. It has been known that the PLL includes a voltage-controlled oscillator whose output frequency is varied correspondingly to an input voltage thereto.

[0003] Since the recent PLL has an on-chip structure due to the recent tendency of increase of the scale of integrated circuit and the operation speed thereof, the voltage-controlled oscillator of such PLL should have a structure suitable to be integrated on a chip. That is, it has been required to develop a voltage-controlled oscillator, which is stable regardless of variation of fabrication process, does not require regulation after fabrication and is durable against noise generated in an integrated circuit.

[0004] In order to realize such voltage-controlled oscillator, a ring oscillator composed of a plurality of differential amplifiers each having a load, by which the ability of the ring oscillator can be controlled, has been proposed in, for example, IEEE Journal of Solid-State Circuits, Vol. 25, No. 6, November, 1990, pp. 1385 to 1394, IEEE Journal of Solid-State Circuits, Vol. 27, No. 11, November, 1992, pp. 1599 to 1607 and U.S. Patent No. 5,412,349. The ring oscillator proposed in each of these articles has characteristics suitable to be integrated on a chip, since the ring oscillator is composed of the differential amplifiers whose sensitivity to power source noise is low, the operating point variation between sampled operating points is small due to simultaneous feedback control of the operating points and the operating point variation due to relative variation within a chip can be made small because an input impedance of the load is low.

[0005] These prior arts will be described in more detail with reference to Figs. 13 to 18. The prior art voltage-controlled oscillator is shown in Fig. 13. In Fig. 13, the voltage-controlled oscillator 103 comprises a ring oscillator 101 and a ring oscillator control circuit 102 for controlling an operation of the ring oscillator.

[0006] Fig. 14 is a block circuit diagram of the ring oscillator 101, which is constructed with differential amplifiers 105 to 108 having identical circuit constructions. Each differential amplifier includes a plus input I1, a minus input I2, a plus output O1, a minus output O2, a current control voltage terminal IC and a load control voltage terminal CL. The differential amplifiers 105 to 108 are connected in series and an output of the differential amplifier 108 is fed back in reverse phase to an input of the differential amplifier 105 to constitute a 4-stage ring oscillator 104. Since the ring oscillator 104 is composed of the differential amplifiers 105 to 108, the sensitivity thereof to power source noise is restricted due to its high ability of removing the power source voltage variation. The current control voltage terminal IC of each differential amplifier has a function of controlling a circuit current thereof and the load control voltage terminal CL thereof has a function of controlling an in-phase output voltage such that the in-phase output voltage is always equal to the reference voltage shown in Fig. 13 by regulating the performance of the load of the differential amplifier.

[0007] Fig. 15 is a circuit diagram of the ring oscillator control circuit 102 shown in Fig. 13. In Fig. 15, an NMOSFET 111 has a gate connected to an oscillation frequency control voltage terminal, which is an input terminal of the voltage-controlled oscillator 103, a source connected to a resistor 110 and a drain connected to a drain of a PMOSFET 112. The gate of the PMOSFET 112 is connected to the drain thereof and a source of the PMOSFET 112 is connected to a power source terminal 115. A differential amplifier 113 has an identical construction to that of each of the differential amplifiers 105 to 108, and input terminals I1 and I2 are commonly connected to the reference voltage terminal and output terminals O1 and O2 are commonly connected to a plus input terminal of a single-end operation amplifier 114. An output terminal of the single-end operation amplifier 114 is connected to a load control voltage terminal CL of the differential amplifier 113. The drain of the PMOSFET 112 is connected to a current control voltage terminal IC of the differential amplifier 113. A minus input terminal of the operation amplifier 114 is connected to the reference voltage source. The operation amplifier 114 controls the voltage of the load control voltage terminal CL of the differential amplifier 113 such that the output voltage of the differential amplifier 113 becomes equal to the reference voltage. Since the differential amplifier 113 has the same construction as that of any of the differential amplifiers 105 to 108, which constitute the ring oscillator 101, and the circuit current and the load control voltage thereof are also the same as those of any one of the differential amplifiers 105 to 108, its in-phase output voltage becomes equal to that of the differential amplifiers 105 to 108.

[0008] Fig. 16 is a circuit diagram of one (121) of the identical differential amplifiers 105 to 108 and 113. In Fig. 16,

the differential amplifier 121 includes an input differential pair of NMOSFET's 124 and 125 and an NMOSFET 126 as a current source. Load circuits 122 and 123 have identical circuit constructions each shown in Fig. 17 or 18. The load circuit shown in Fig. 17 is composed of an NMOSFET 132 having a gate supplied with a load control voltage and an NMOSFET 133 having a gate and a drain connected to the gate thereof. A terminal 131 is connected to one of the output terminals O1 and O2 shown in Fig. 16. Since the gate of the NMOSFET 133 is connected to an output terminal 131, an impedance looked from the terminal 131 of the NMOSFET 133, that is, an output impedance, is in inverse proportion to a mutual conductance of the NMOSFET 133 and has a low value. Further, since the NMOSFET 132 having the gate supplied with the load control voltage operates in a saturation region, when the load control voltage is low and the following relation is established between the voltage V_o at the output terminal 131 and the load control voltage V_{CL} :

$$V_{CL} - V_{th} < V_o$$

where V_{th} is the threshold voltage of the NMOSFET 132. Therefore, the output impedance of the load becomes very large. That is, the output impedance is represented by $\Delta V/\Delta i$, a ratio of voltage change ΔV to current change Δi . In the saturation region, since current i is substantially constant, Δi is very close to 0 and the output impedance becomes substantially infinite. However, in order to make the in-phase output voltage constant even when the operating current is changed, the NMOSFET 132 whose performance can be controlled by the load control voltage is indispensable. That is, it is impossible to control the in-phase output voltage by only the NMOSFET 133 since the in-phase output voltage is varied by the operating current. Consequently, it becomes possible by using both the NMOSFET's 132 and 133 to reduce the output impedance of the load to a low value and to make the in-phase output voltage constant.

[0009] The load circuit shown in Fig. 18 includes, in addition to the NMOSFET's 132 and 133 shown in Fig. 17, an NMOSFET 134 having a gate supplied with the load control voltage and provided on the source side of the NMOSFET 133. In the load circuit shown in Fig. 17, when the operating current is reduced and a substantial portion of the operating current flows through the NMOSFET 133, an amplitude of the oscillation frequency output is reduced in a range of operating current smaller than the operating current. In the load circuit shown in Fig. 18, such phenomenon does not occur due to the provision of the NMOSFET 134.

[0010] In this case, however, since an output impedance of the series circuit including the NMOSFET's 133 and 134 is determined by the NMOSFET 134, the output impedance of the series-connected NMOSFET's 133 and 134 becomes very large when the NMOSFET 134 operates in the saturation region. As a result, there is a lower limit of the output frequency range of the voltage-controlled oscillator 103 constituted with the differential amplifiers 121.

[0011] Now, the reason for the necessity of maintaining the in-phase output voltage at constant will be described. In order to connect the voltage-controlled oscillator to a usual CMOS digital circuit, it is necessary to convert the differential output of the ring oscillator 101, that is, the voltage-controlled oscillator 103, into a single-ended CMOS level. In order to realize such conversion, it is necessary to stabilize the in-phase output voltage of the differential output of the voltage-controlled oscillator 103, otherwise, a circuit for converting the differential output into the single-ended CMOS level does not operate normally or, if it operates normally, the operating speed and/or the duty cycle may be degraded.

[0012] The purpose of reduction of the output impedances of the loads is to prevent the operating points of the differential amplifiers 105 to 108 from being substantially varied due to relative variation between the current source transistors 126 of the differential amplifiers 105 to 108 and 113 and transistors constituting the load circuits and to restrict the influence of coupling through other wiring and/or a silicon substrate of the integrated circuit.

[0013] As mentioned, although the voltage-controlled oscillator including the ring oscillator constituted with the differential amplifiers 121 each having the load circuit shown in Fig. 17 or 18 has characteristics suitable for circuit integration, the range of oscillation frequency thereof is narrow. Therefore, it is difficult to use the prior art voltage-controlled oscillator for the PLL of the disk servo system of such as CD-ROM, which requires the output frequency range from several to ten times the reference frequency.

[0014] Further, although the load circuit shown in Fig. 17 or 18 includes a transistor having a gate short-circuited to a drain thereof, the in-phase output voltage of the differential amplifier must be high enough when the threshold value of the transistor is high. However, when the in-phase output voltage is high, the paired differential transistors 124 and 125 are not saturated, so that it becomes impossible to obtain a voltage gain. Therefore, it is necessary to sufficiently reduce the in-phase output voltage of the differential amplifier 121. Accordingly, special fabrication steps dedicated thereto must be added in order to reduce the threshold voltage of the transistors constituting the load circuit.

SUMMARY OF THE INVENTION

[0015] An object of the present invention is to provide a voltage-controlled oscillator having a wide oscillation output frequency range, which can be fabricated without adding any special fabrication step to a usual fabrication method of a voltage-controlled oscillator.

[0016] In order to achieve the above object, a voltage-controlled oscillator according to a first aspect of the present

invention includes a ring oscillator constituted with a plurality of differential amplifiers each having a first input terminal, a second input terminal, a first output terminal, a second output terminal and a current limiting terminal, the first and second input terminals of the differential amplifiers being ring-connected to the corresponding first and second output terminals of the differential amplifiers, a first load circuit connected to each of the first output terminal, a second load circuit connected to each second output terminal and is featured by that the first and second load circuits always operate in a linear region.

[0017] A voltage-controlled oscillator according to a second aspect of the present invention includes a ring oscillator constituted with a plurality of differential amplifiers each having a first input terminal, a second input terminal, a first output terminal, a second output terminal and a current limiting terminal, the first and second input terminals of the differential amplifiers being ring-connected to the corresponding first and second output terminals of the differential amplifiers, a first load circuit connected to each of the first output terminal and supplied with a first and second load control voltages, a second load circuit connected to each second output terminal and supplied with the first and second load control voltages and is featured by that the first and second load circuits always operate in a linear region according to the first and second load control voltages.

[0018] With such circuit construction of the voltage-controlled oscillator, an output impedance of the differential amplifiers is always restricted to a low level, so that it is possible to widen the oscillation frequency thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The above-mentioned and other objects, features and advantages of the present invention will become more apparent by reference to the following detailed description of the invention taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block circuit diagram of a voltage-controlled oscillator according to a first embodiment of the present invention;

Fig. 2 is a block circuit diagram of a ring oscillator shown in Fig. 1;

Fig. 3 is a circuit diagram of a ring oscillator control circuit shown in Fig. 1;

Fig. 4 is a circuit diagram of a differential amplifier shown in Fig. 2 or 3;

Fig. 5 is a circuit diagram of a load circuit shown in Fig. 4;

Fig. 6 is a block circuit diagram of a voltage-controlled oscillator according to a second embodiment of the present invention;

Fig. 7 is a block circuit diagram of a ring oscillator shown in Fig. 6;

Fig. 8 is a circuit diagram of a ring oscillator control circuit shown in Fig. 6;

Fig. 9 is a circuit diagram of a differential amplifier shown in Fig. 7 or 8;

Fig. 10 is a circuit diagram of a load circuit shown in Fig. 9;

Fig. 11 is a circuit diagram of a modification of the ring oscillator shown in Fig. 8;

Fig. 12 is a circuit diagram of a modification of the load circuit shown in Fig. 9;

Fig. 13 is a block circuit diagram of a conventional voltage-controlled oscillator;

Fig. 14 is a block circuit diagram of a ring oscillator shown in Fig. 13;

Fig. 15 is a circuit diagram of a ring oscillator control circuit shown in Fig. 13;

Fig. 16 is a circuit diagram of a differential amplifier shown in Fig. 14 or 15;

Fig. 17 is a circuit diagram of a load circuit shown in Fig. 16; and

Fig. 18 is a circuit diagram of another load circuit shown in Fig. 16.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0020] A voltage-controlled oscillator according to a first embodiment of the present invention will be described with reference to Fig. 1.

[0021] In Fig. 1, a voltage-controlled oscillator 3 includes a ring oscillator control circuit 2 supplied with an oscillation frequency control voltage and a reference voltage and a ring oscillator 1 supplied with a current control voltage and load control voltages 1 and 2, which are outputted by the ring oscillator control circuit 2. An output of the ring oscillator 1 becomes an output of the voltage-controlled oscillator 3. Fig. 2 is a circuit diagram of the ring oscillator 1 shown in Fig. 1. The ring oscillator 1 is constituted with a plurality of differential amplifiers, in this embodiment, four differential amplifiers 5 to 8, each having a plus input terminal I1, a minus input terminal I2, a plus output terminal O1, a minus output terminal O2, a current control voltage terminal IC and a pair of load control voltage terminals CL1 and CL2. The differential amplifiers 5 to 8 are connected in series in this order and the outputs at the output terminals O1 and O2 of the differential amplifier 8 are fed back to the inputs of the differential amplifier 5 in inverse phase to constitute a 4-stage ring oscillator. The oscillation frequency of the ring oscillator 1 is controlled by changing an operating current thereof by

a current control voltage supplied to the current control voltage terminal IC while regulating the in-phase output voltage thereof constant by the load control voltage at the load control voltage terminals CL1 and CL2. Although the shown ring oscillator has the 4-stage construction, it has been well known that the ring oscillator can function as an oscillator when there are at least 3-stage construction.

5 **[0022]** The differential amplifiers 5 to 8 have identical constructions, one of which is shown as a differential amplifier 21 in Fig. 4. As shown in Fig. 4, the differential amplifier 21 includes load circuits 22 and 23 supplied with load control voltages 1 and 2 from the load control voltage terminals CL1 and CL2, a differential pair of PMOSFET's 24 and 25 having gates connected to the input terminals I1 and I2 and drains connected to the output terminals O2 and O1, respectively, and a PMOSFET 26 having a gate connected to the current control terminal IC and a source connected to the power source line 18 to constitute a current source.

10 **[0023]** As shown in Fig. 5, each of the load circuits 22 and 23 of the differential amplifier shown in Fig. 4 includes an NMOSFET 32 having a gate supplied with the load control voltage 1 and an NMOSFET 33 having a gate supplied with the load control voltage 2. Assuming that (gate width)/(gate length) of the NMOSFET 32 is K32 and (gate width)/(gate length) of the NMOSFET 33 is K33, K32 is set equal to or larger than K33. An output terminal 31 of the load circuit 22 is connected to the drain of the PMOSFET 24 and an output terminal 31 of the load circuit 23 is connected to the drain of the PMOSFET 25.

15 **[0024]** A construction of the ring oscillator control circuit 2 shown in Fig. 1 is shown in Fig. 3. As shown in Fig. 3, the ring oscillator control circuit 2 includes an NMOSFET 16 having a gate supplied with the oscillation frequency control voltage, which is the input terminal of the voltage-controlled oscillator, a resistor 15 connected between ground and a source of the NMOSFET 16, a PMOSFET 17 having a drain and a gate, both of which are commonly connected to a drain of the NMOSFET 16, and a source connected to the voltage source line 18, a differential amplifier 19 having a current control terminal IC supplied with a current control voltage generated at a junction between the PMOSFET 17 and the NMOSFET 16, an operation amplifier 20 having a plus input supplied with an output of the differential amplifier 19 and outputting the load control voltage 1 and a voltage amplifier 10 supplied with the load control voltage 1 and outputting the load control voltage 2. The operating currents of the differential amplifiers 5 to 8 are controlled by the current control voltage supplied to the current control terminals IC thereof.

20 **[0025]** The differential amplifier 19 may be any provided that it outputs a voltage equal to the in-phase output voltage of one of the differential amplifiers 5 to 8. In this embodiment, however, the differential amplifier 19 has a circuit construction identical to that of one of the differential amplifiers 5 to 8 and has a plus and a minus inputs terminals I1 and I2 commonly supplied with the reference voltage, which is the input of the voltage-controlled oscillator 3, and output terminals O1 and O2 connected commonly to the plus input of the operational amplifier 20. Alternatively, the differential amplifier 19 may take other constructions. For example, the differential amplifier 19 may have the same circuit construction as that of the differential amplifier 21 shown in Fig. 4 with the gate width of the current source 26 being made 1/2 and the load circuit 23 and the transistor 25 being removed. Alternatively, the differential amplifier 19 may have the same circuit construction as that of the differential amplifier 21, with the PMOSFET's 24 and 25 being removed and the PMOSFET 26 being directly connected to the load circuits 22 and 23. In the latter case, the reference voltage is not supplied thereto.

25 **[0026]** The voltage amplifier 10 is constituted with an NMOSFET 11 having a source grounded and a gate supplied with the load control voltage 1, a PMOSFET 12 having a source connected to the voltage source line 18 and a gate and a drain, which are commonly connected to a drain of the NMOSFET 11, a PMOSFET 13 having a source connected to the voltage source line 18 and a gate connected to the gate of the PMOSFET 12 and an NMOSFET 14 having a source grounded and a drain and a gate, which are commonly connected to a drain of the PMOSFET 13. A drain voltage of the NMOSFET 14 is outputted as the load control voltage 2. The load control voltage 2 is supplied to the differential amplifier 19 and the differential amplifiers 5 to 8 constituting the ring oscillator 1.

30 **[0027]** An operation of the voltage-controlled oscillator 3 according to this embodiment will be described.

[0028] The voltage-controlled oscillator 3 outputs an oscillation frequency, which is controlled by the oscillation frequency control voltage inputted to the ring oscillator control circuit 2, as shown in Fig. 1. In the circuit shown in Fig. 1, the oscillation frequency is increased with increase of the oscillation frequency control voltage. This operation will be described first.

35 **[0029]** The operating current of each of the differential amplifier 19 and the differential amplifiers 5 to 8 is supplied from the current source, that is, the PMOSFET 26 having the gate supplied with the IC terminal voltage, and is determined by the Miller effect of a current flowing through a source-drain circuit of the PMOSFET 17 shown in Fig. 3. The current flowing through the source-drain circuit of the PMOSFET 17 is the same as a current flowing through the resistor 15. The current flowing through the resistor 15 is substantially zero when the oscillation frequency control voltage is equal to or lower than the threshold voltage of the NMOSFET 16. It is well known that, when the oscillation frequency control voltage exceeds the threshold voltage of the NMOSFET 16, the current flowing through the resistor 15 becomes substantially proportional to a current represented by the following formula:

$$\{(\text{oscillation frequency control voltage}) - (\text{threshold voltage of NMOSFET 16})\}/R \quad (1)$$

where R is a resistance value of the resistor 15. Therefore, the operating current of each of the differential amplifiers 5 to 8 and 19 is substantially proportional to the formula (1).

5 [0030] Incidentally, the oscillation frequency of the ring oscillator 1 is represented by the following formula:

$$1/(2\pi CLRL) \quad (2)$$

where CL is a load capacitance of the outputs O1 and O2 of each of the differential amplifiers 5 to 8, which includes drain junction capacitances of the PMOSFET's 24 and 25 and the NMOSFET's 32 and 33, which constitute the load circuits 22 and 23, gate capacitances of the PMOSFET's 24 and 25 of a next stage and a capacitance of a wiring and RL is an output impedance of the output O1 and O2, which is a sum of output impedances of the load circuit 22 and the PMOSFET 24 or a sum of output impedances of the load circuit 23 and the PMOSFET 25. The reason for that the oscillation frequency is given by the formula (2) will be described. The oscillation frequency given by the formula (2) is a first pole frequency of the differential amplifiers 5 to 8 and a phase of the output of the differential amplifiers 5 to 8 is rotated by 45° at this frequency. Further, the oscillation occurs at a frequency at which the phase from the input to the differential amplifier 5 to the output of the differential amplifier 8 is rotated by 180° and, since the ring oscillator 1 has the 4-stage construction, the oscillation occurs at a frequency whose phase for one stage is rotated by 45°. Therefore, the ring oscillator 1 oscillates at the first pole frequency. Needless to say, RL is reduced when the circuit current increases. Therefore, since the operating current is substantially proportional to the formula (1), the output frequency of the voltage-controlled oscillator 3 increases when the oscillation control voltage becomes high. Since there is no current flows when the oscillation frequency control voltage is in the ground potential level, the oscillation is terminated. Although an oscillation frequency of a ring oscillator having other construction than 4-stage construction is given by a formula different from the formula (2), the oscillation frequency can be obtained in a similar manner and the output frequency of the voltage-controlled oscillator also increases with increase of the oscillation frequency control voltage.

25 [0031] Now, the reason for that the output impedance of the differential amplifiers 5 to 8 constituting the ring oscillator 1 of this embodiment can be reduced will be described. First, a relation between the load control voltage 1 and the load control voltage 2 in Fig. 2 will be described. Here, it is assumed that, in Fig. 3, (gate width)/(gate length) ratios of the NMOSFET's 11, 12 and the PMOSFET's 13 and 14 are represented by K11, K12, K13 and K14, respectively, the threshold voltages of the NMOSFET's 11 and 14 are commonly Vtn and the threshold voltages of the PMOSFET's 12 and 13 are commonly Vtp. The MOSFET's 11 to 14 are set to operate in saturation regions respectively. In such case, currents I11 to I14 flowing through the MOSFET's 11 to 14 are given by the following formulas, respectively:

$$I_{11} = \mu_n C_{ox} K_{11} (V_{gsn11} - V_{tn})^2/2 \quad (3)$$

$$I_{12} = \mu_n C_{ox} K_{12} (V_{gsp} - V_{tp})^2/2 \quad (4)$$

$$I_{13} = \mu_n C_{ox} K_{13} (V_{gsp} - V_{tp})^2/2 \quad (5)$$

$$I_{14} = \mu_n C_{ox} K_{14} (V_{gsn14} - V_{tn})^2/2 \quad (6)$$

where μ_n and μ_p are mobilities of electron and hole in silicon, C_{ox} is a gate capacitance for unit area, V_{gsn11} is a voltage between the gate and the source of the NMOSFET 11, V_{gsp} is a voltage between the gate and the source of the PMOSFET 12 as well as the PMOSFET 13 and V_{gsn14} is a voltage between the gate and the source of the NMOSFET 14. Since the gates of the PMOSFET's 12 and 13 are common and the sources thereof are commonly connected to the voltage source 18, the voltages between the gates and the sources thereof are equal each other. Further, since currents flowing through the NMOSFET 11 and the PMOSFET 12 are the same and currents flowing through the PMOSFET 13 and the NMOSFET 14 are the same, the following formulas are established:

$$I_{11} = I_{12} \quad (7)$$

$$I_{13} = I_{14} \quad (8)$$

From the formulas (3) to (8), the following formula is obtained:

$$V_{gsn14} - V_{tn} = \{K_{11} K_{13}/(K_{12} K_{14})\}^{1/2} (V_{gsn11} - V_{tn}) \quad (9)$$

From the formula (9), it is clear that $(V_{gsn14} - V_{tn})$ is always equal to $(V_{gsn11} - V_{tn})$ multiplied with

{K11K13/(K12K14)}^{1/2}. For example, when K11 is twice K12 and K13 is twice K14, the voltage (V_{gsn14} - V_{tn}) is always twice the voltage (V_{gsn11} - V_{tn}). That is, by setting K11 to K14, which are ratios of the gate widths to the gate lengths of the respective MOSFET's 11 to 14, to suitable values, it is possible to always make the difference between the load control voltage 2 and V_{tn} a constant number multiple of the difference between the load control voltage 1 and V_{tn}. Therefore, it is possible, in the load circuits 22 and 23, which are constituted with the NMOSFET's 32 and 33, respectively, to arbitrarily make the voltage between the gate and the source of the NMOSFET 33 higher than the voltage between the gate and the source of the NMOSFET 32. Consequently, it is possible to operate the NMOSFET 33 in a linear region even when the voltage value of the load control voltage 1 allows the NMOSFET 32 to operate in the saturation region. It has been known that the operation region of the NMOSFET 32 or 33 is determined by

$$(\text{voltage between gate and source}) - (\text{threshold voltage})$$

since, in this embodiment, the in-phase output voltage is fixed to the reference voltage. Since it is possible to set this voltage of the NMOSFET 33 to an arbitrary high value according to the formula (9), it is possible to make the load control voltage 2 to a value with which the NMOSFET 33 operates in the linear region by setting the values of K13 and K14, even when the oscillation frequency control voltage is low and the load control voltage 1 is low enough to operate the NMOSFET 32 in the saturation region. Incidentally, same operation can be obtained by using a voltage amplifier having high voltage gain preciseness instead of the voltage amplifier 10.

[0032] Further, it is necessary to make the driving ability of one of the NMOSFET's 32 and 33 constituting the respective load circuits 22 and 23, which reaches the saturation region first, smaller than that of the other, which is operating in the linear region. This is because, if the driving ability of the NMOSFET operating in the saturation region becomes dominant, the output impedance of the NMOSFET operating in the linear region does not attribute substantially to the output impedance of the output 31 of the load circuit, so that the output impedance of the output 31 of the load circuit becomes large. Therefore, it is enough to make the gate width of the NMOSFET operating in the linear region larger than that of the NMOSFET operating in the saturation region. Since the gate width can be made large by connecting NMOSFET's in parallel, without increasing the number of fabrication steps.

[0033] A second embodiment of the present invention is shown in Figs. 6 to 10. The basic construction of the second embodiment is the same as that of the first embodiment, except that the load circuit includes n transistors connected in parallel as shown in Fig. 10 and n load control voltages are provided correspondingly to the n transistors, as shown in Fig. 10, where n is an integer larger than 2. The n load control voltages are generated by a ring oscillator control circuit, which includes (n-1) voltage amplifiers 50 each identical to the voltage amplifier 10 shown in Fig. 3, as shown in Fig. 8. Assuming that values obtained for the respective n load control voltages according the formula {K11K13/(K12K14)}^{1/2} determining the voltage amplification obtained in the first embodiment are $\alpha_1, \alpha_2, \dots, \alpha_{n-1}$, these values are set in this embodiment as follow:

$$\alpha_1 < \alpha_2 < \dots < \alpha_{n-1}$$

That is, the load control voltages are set in such a way of (load control voltage 1) < (load control voltage 2) < ... < (load control voltage n).

[0034] With such circuit construction, it is possible to operate any one of the transistors constituting the load circuit in the linear region within a wider operating current range than that of the first embodiment. That is, it is possible to reduce the output impedance of the differential amplifiers constituting the ring oscillator in the wider operating current range to thereby obtain the voltage-controlled oscillator having a wider stable oscillation frequency range.

[0035] It is further effective when the driving ability of the transistors is changed such that the driving ability of transistors operating in the saturation region becomes smaller than that of the transistors operating in the linear region.

[0036] The ring oscillator control circuit shown in Fig. 8 may be replaced by a ring oscillator control circuit shown in Fig. 11. In such case, the number of transistors can be reduced, compared with the ring oscillator control circuit shown in Fig. 8. The ring oscillator control circuit shown in Fig. 11 operates in a similar manner to the ring oscillator control circuit shown in Fig. 8 by replacing the values of K13 and K14 of the formula {K11K12/(K13K14)}^{1/2} obtained for the load circuit 10 shown in Fig. 3 by those corresponding to the respective transistors.

[0037] Fig. 12 shows a modification of the load circuit shown in Fig. 10, in which an NMOSFET 90 is added to the load circuit shown in Fig. 10. This modification can realize a voltage-controlled oscillator, which can operate similarly to the voltage-controlled oscillator shown in Fig. 6. When the circuit shown in Fig. 12 is used, it is possible to reduce the output impedance due to the provision of the NMOSFET 90, with a small operating current with which all of the transistors of the load circuit shown in Fig. 10 may operate in the saturation region and the output impedance may be increased. Therefore, it is possible to solve the problem of the load circuit shown in Fig. 10 that the oscillation is stopped due to a relative variation of operations of the transistors when the operating current is small enough to operate all of the transistors thereof in the saturation region. Consequently, even if the in-phase output voltage is lowered and the pre-

ciseness, etc., of the operation is degraded, it is possible to reliably obtain the oscillation output.

[0038] According to the present invention, it is possible to provide a voltage-controlled oscillator capable of stably oscillating in a wide frequency range. By increasing the number of parallel-connected load transistors of the load circuit to increase the number of load control voltages, it is possible to arbitrarily widen the oscillation frequency range of the voltage-controlled oscillator. Since the reference voltage of the voltage-controlled oscillator can be set to a low value compared with that of the conventional oscillator, the transistors constituting the load circuit can be easily operated in the linear region, so that it is easier to reduce the output impedance of the differential amplifiers constituting the ring oscillator. With the latter advantage, the operating current range can be widened.

[0039] Further, it is possible to realize a voltage-controlled oscillator regardless of the voltage value of the reference voltage, which is the input for determining the in-phase output voltage, and regardless of the threshold voltages of the MOSFETs.

Claims

1. A voltage-controlled oscillator comprising a ring oscillator including a plurality of differential amplifiers each having a first input terminal, a second input terminal, a first output terminal, a second output terminal and a current limiting terminal, said first and second input terminals of the plurality of said differential amplifiers and said first and second output terminals of said differential amplifiers corresponding thereto being ring-connected, each said differential amplifier comprising a first load circuit connected to said first output terminal thereof and a second load circuit connected to said second output terminal thereof, said first and second load circuits operating always in a linear operating region.
2. A voltage-controlled oscillator as claimed in claim 1, wherein each said differential amplifier comprises a first transistor connected between a first power source line and a first node and having a gate supplied with a current control voltage, a second transistor connected between said first node and said first input terminal thereof and having a gate supplied with a first input signal, a third transistor connected between said first node and said second input terminal thereof and having a gate supplied with a second input signal, said first load circuit connected between said first node and a second power source line and said second load circuit connected between said first node and said second power source line.
3. A voltage-controlled oscillator as claimed in claim 2, wherein said first load circuit comprises a fourth transistor connected between said first input terminal thereof and said second power source line and having a gate supplied with a first load control voltage and a fifth transistor connected between said first input terminal thereof and said second power source line and having a gate supplied with a second load control voltage and wherein said second load circuit comprises a sixth transistor connected between said second input terminal thereof and said second power source line and having a gate supplied with the first load control voltage and a seventh transistor connected between said second input terminal thereof and said second power source line and having a gate supplied with the second load control voltage.
4. A voltage-controlled oscillator as claimed in claim 3, wherein the current amplification of said fourth transistor is different from the current amplification of said fifth transistor and the current amplification of said sixth transistor is different from the current amplification of said seventh transistor.
5. A voltage-controlled oscillator as claimed in claim 3, wherein the gate width/gate length ratio of said fourth transistor is different from the gate width/gate length ratio of said fifth transistor and the gate width/gate length ratio of said sixth transistor is different from the gate width/gate length ratio of said seventh transistor.
6. A voltage-controlled oscillator as claimed in claim 3, further comprising a ring oscillator control circuit responsive to an oscillation frequency control voltage for generating the first load control voltage and the second load control voltage different from the first load control voltage.
7. A voltage-controlled oscillator as claimed in claim 6, wherein said ring oscillator control circuit comprises a first load control voltage generator circuit responsive to the oscillation frequency control voltage and the reference voltage for generating the first load control voltage and a second load control voltage generator circuit responsive to the first load control voltage for generating the second load control voltage proportional to the first load control voltage.
8. A voltage-controlled oscillator comprising a ring oscillator including a plurality of differential amplifiers each having a first input terminal, a second input terminal, a first output terminal, a second output terminal and a current limiting

terminal, said first and second input terminals of the plurality of said differential amplifiers and said first and second output terminals of said differential amplifiers corresponding thereto being ring-connected, each said differential amplifier comprising a first load circuit connected to said first output terminal thereof and receiving a load control voltage and a second load circuit connected to said second output terminal thereof and receiving the first and second load control voltages, said first and second load circuits responsive to the first and second load control voltages for operating always in a linear operating region.

9. A voltage-controlled oscillator as claimed in claim 8, further comprising a load control voltage generator circuit for generating the first load control voltage and the second load control voltage different from the first load control voltage.

10. A voltage-controlled oscillator as claimed in claim 9, wherein said first load circuit comprises a first transistor connected between the first output terminal and a first power source line and having a gate supplied with the first load control voltage and a second transistor connected between said first output terminal and said first power source line and having a gate supplied with the second load control voltage, said second load circuit comprises a third transistor connected between said second output terminal and said first power source line and having a gate supplied with the first load control voltage and a fourth transistor connected between said second output terminal and said first power source line and having a gate supplied with the second load control voltage, wherein the first and second load control voltages are supplied such that, when said first and third transistors are in saturation region, said second and fourth transistors are in linear region.

Fig.1

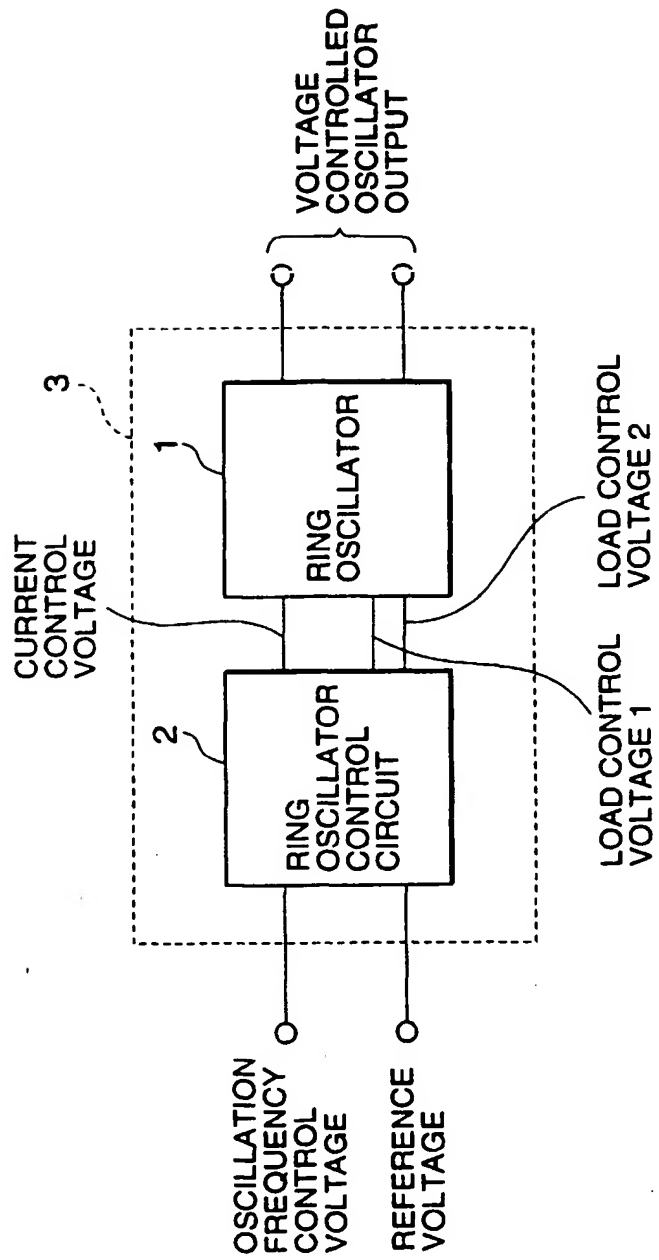


Fig.2

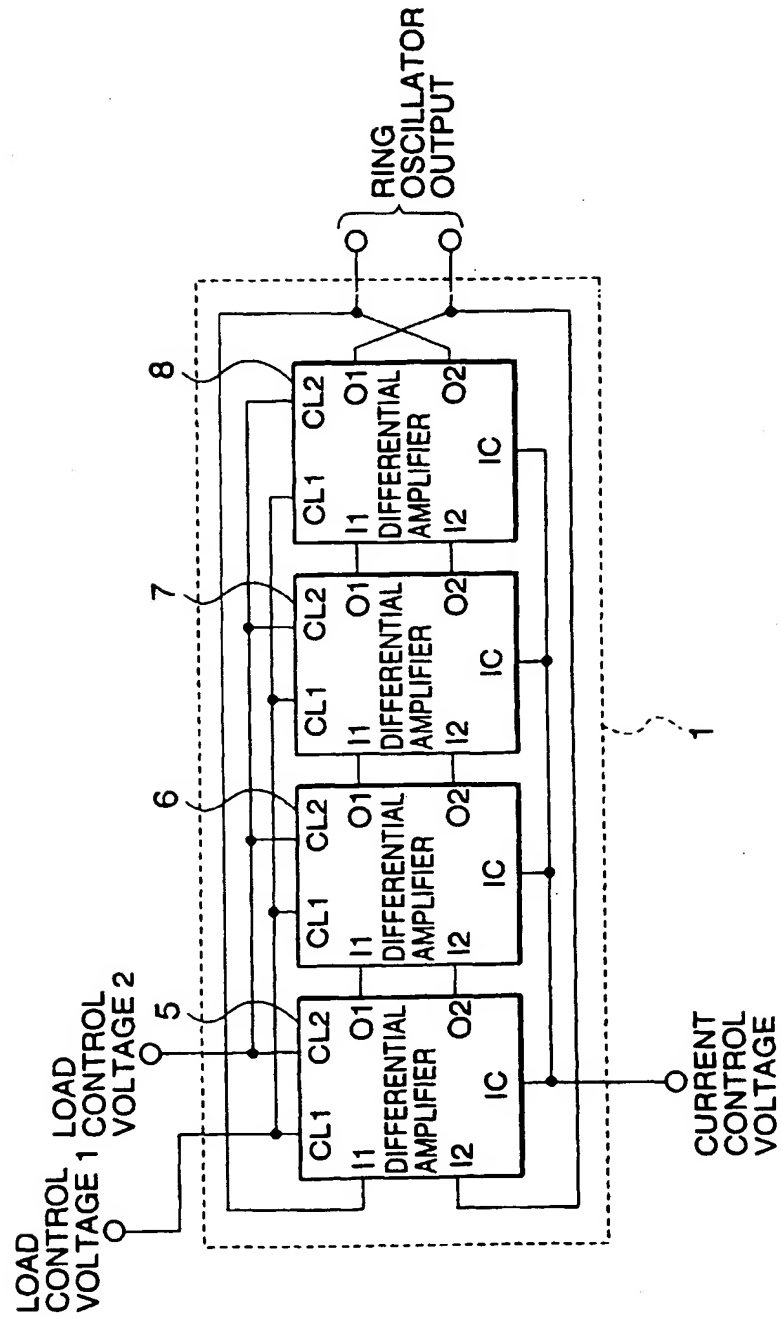


Fig.3

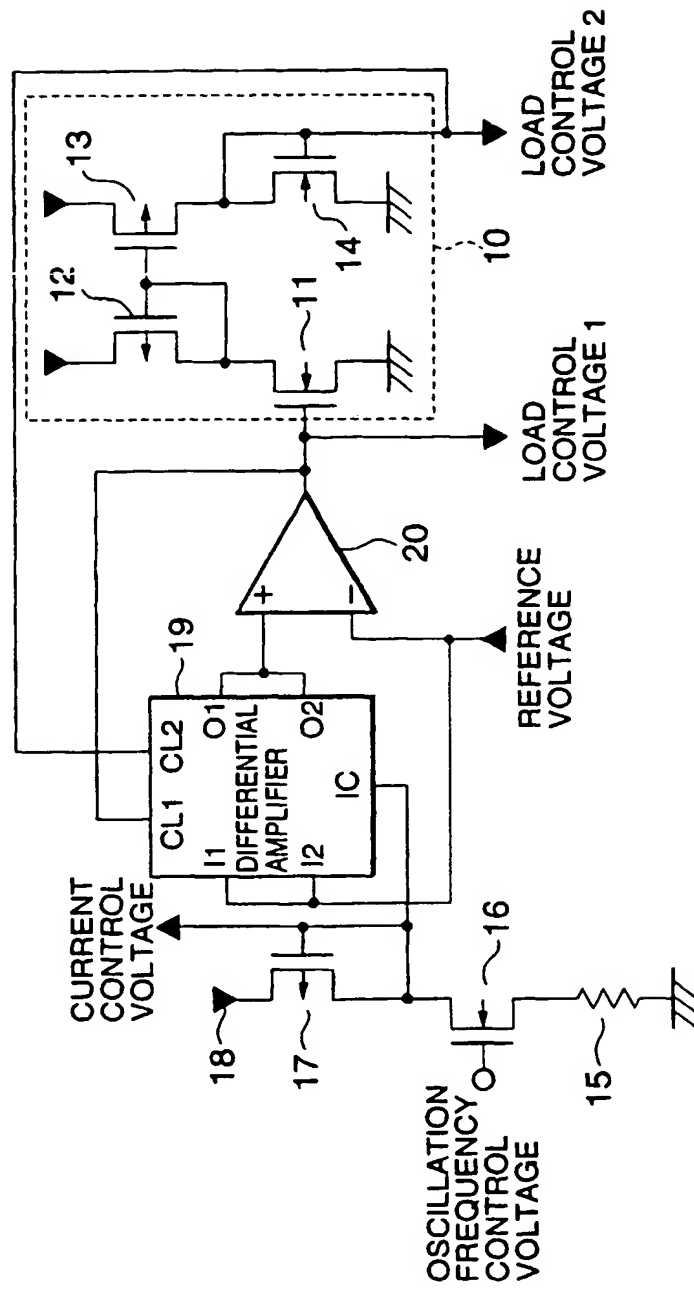


Fig.4

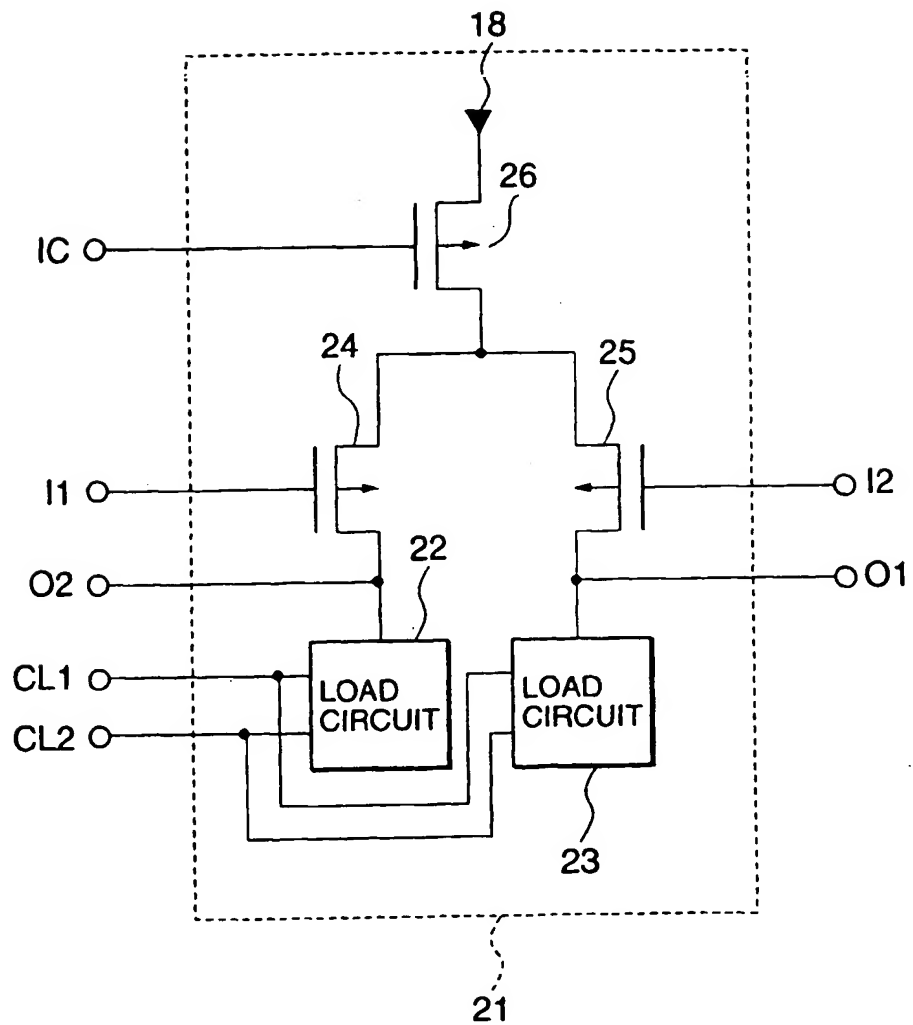


Fig.5

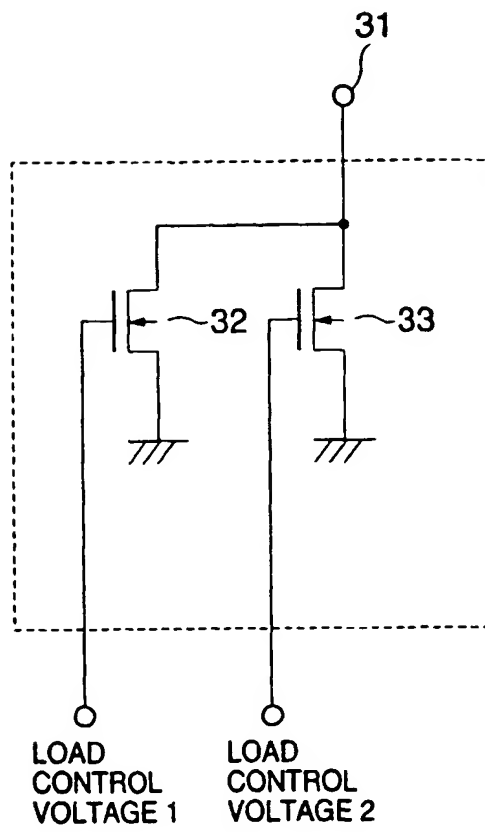


Fig.6

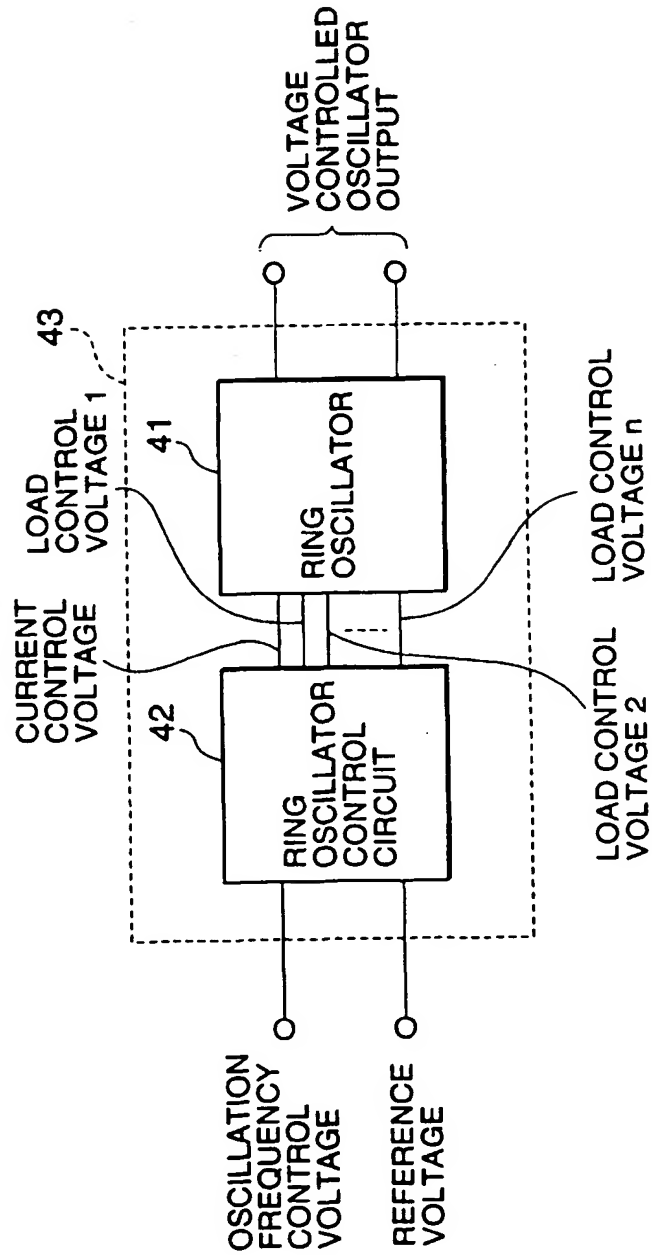


Fig.7

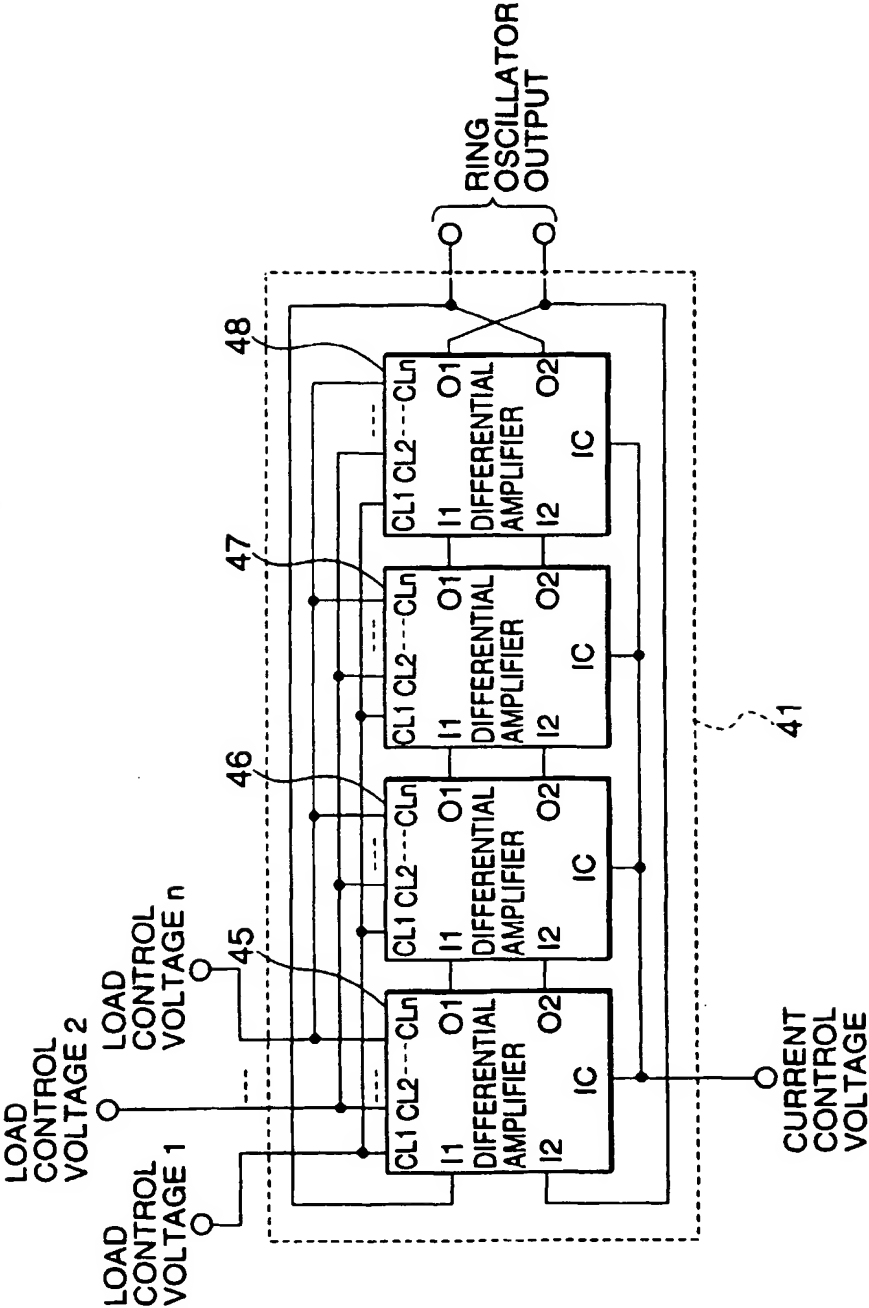


Fig.8

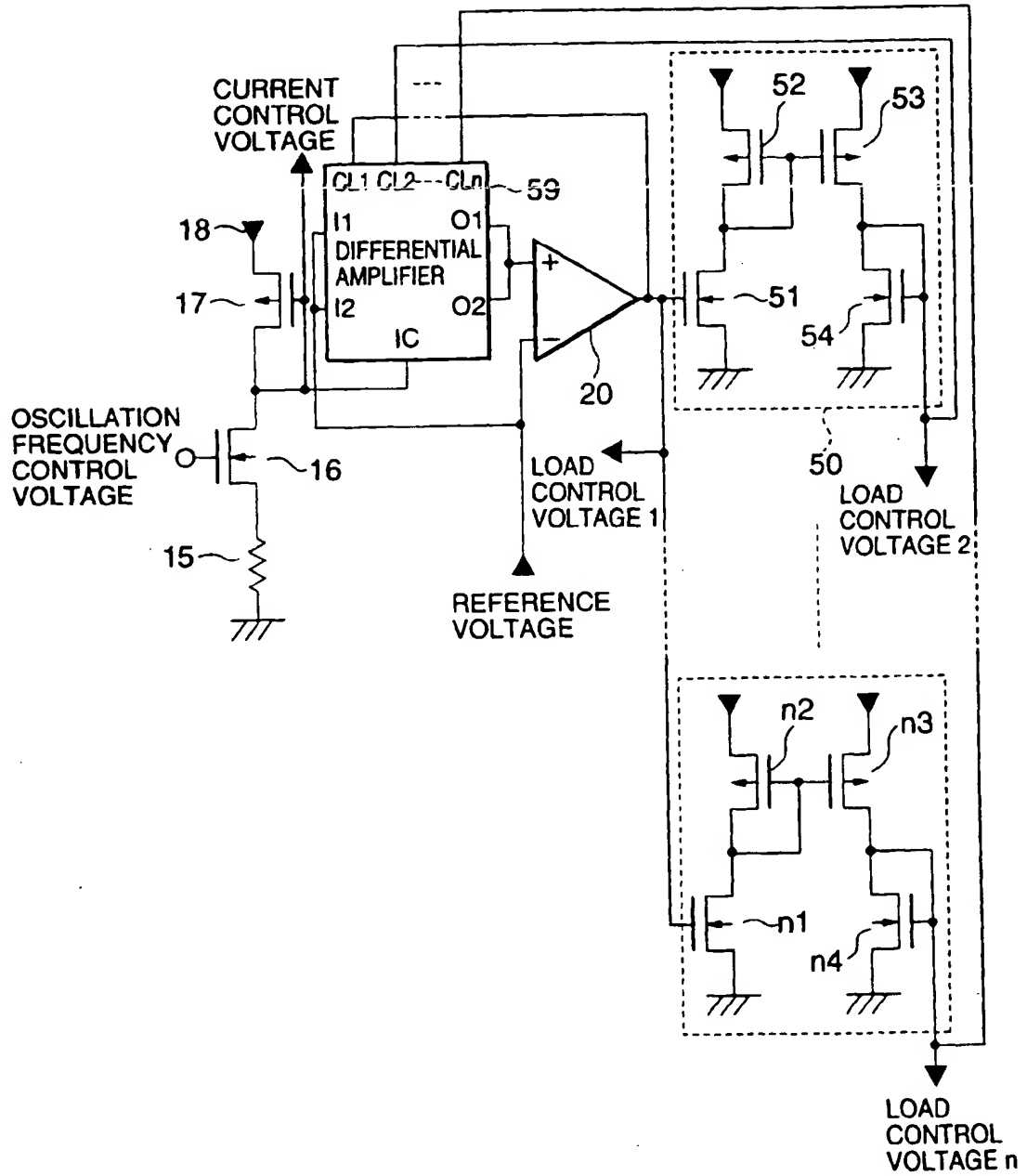


Fig.9

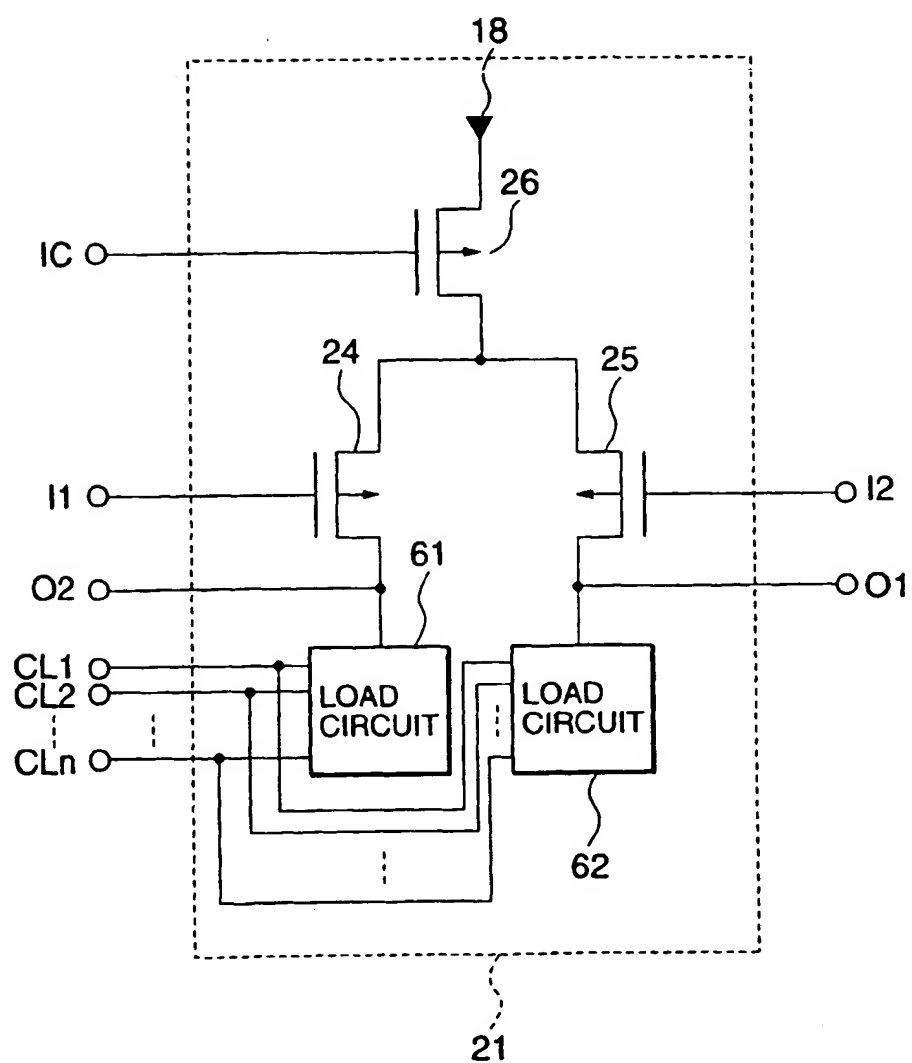


Fig.10

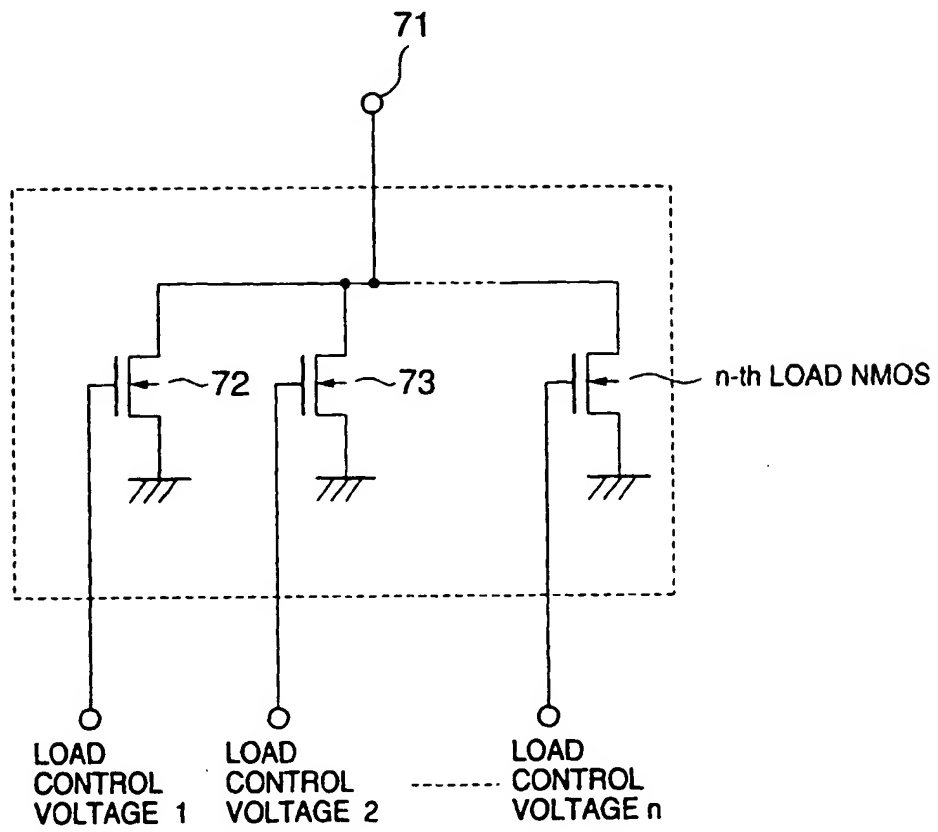


Fig.11

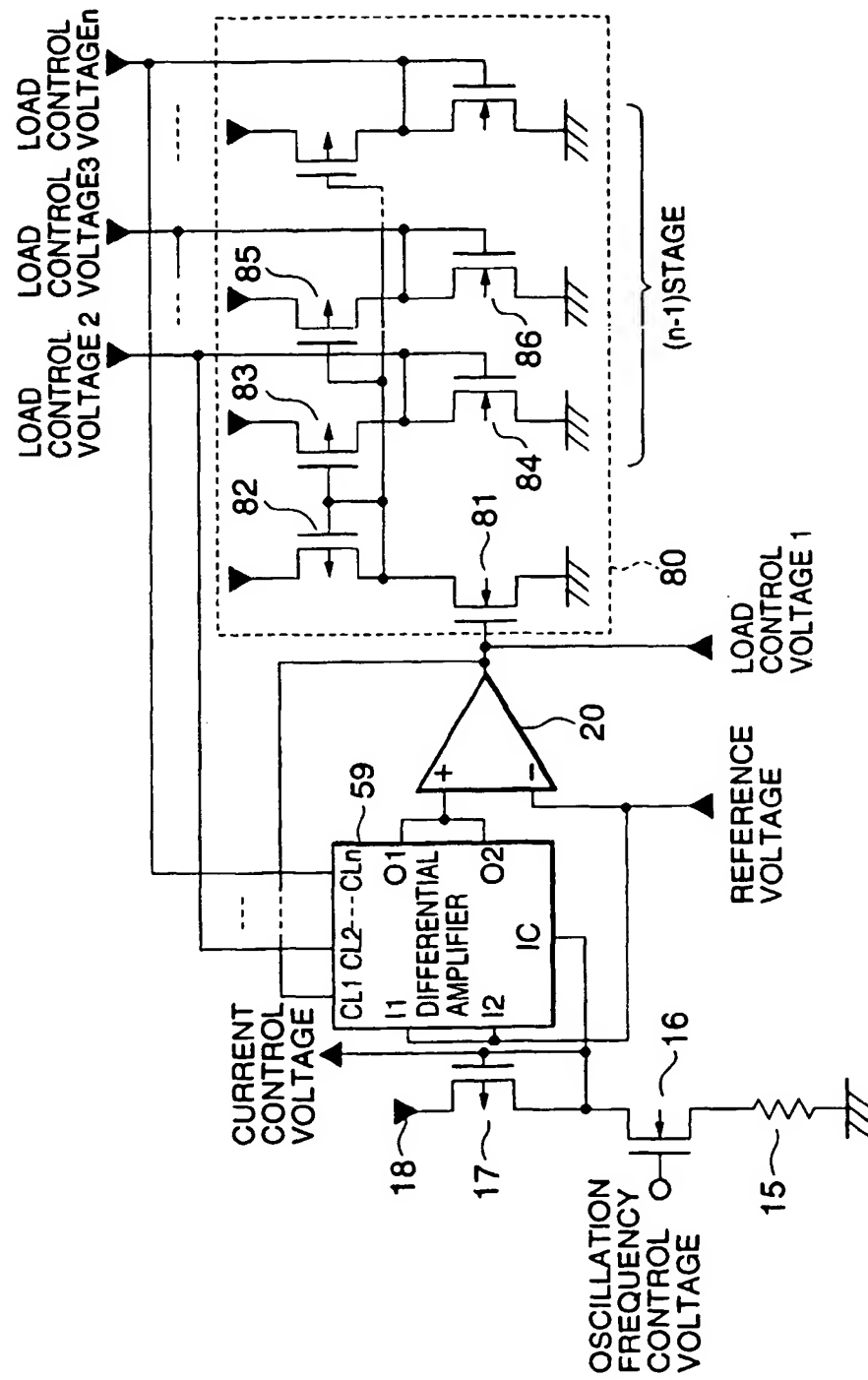


Fig.12

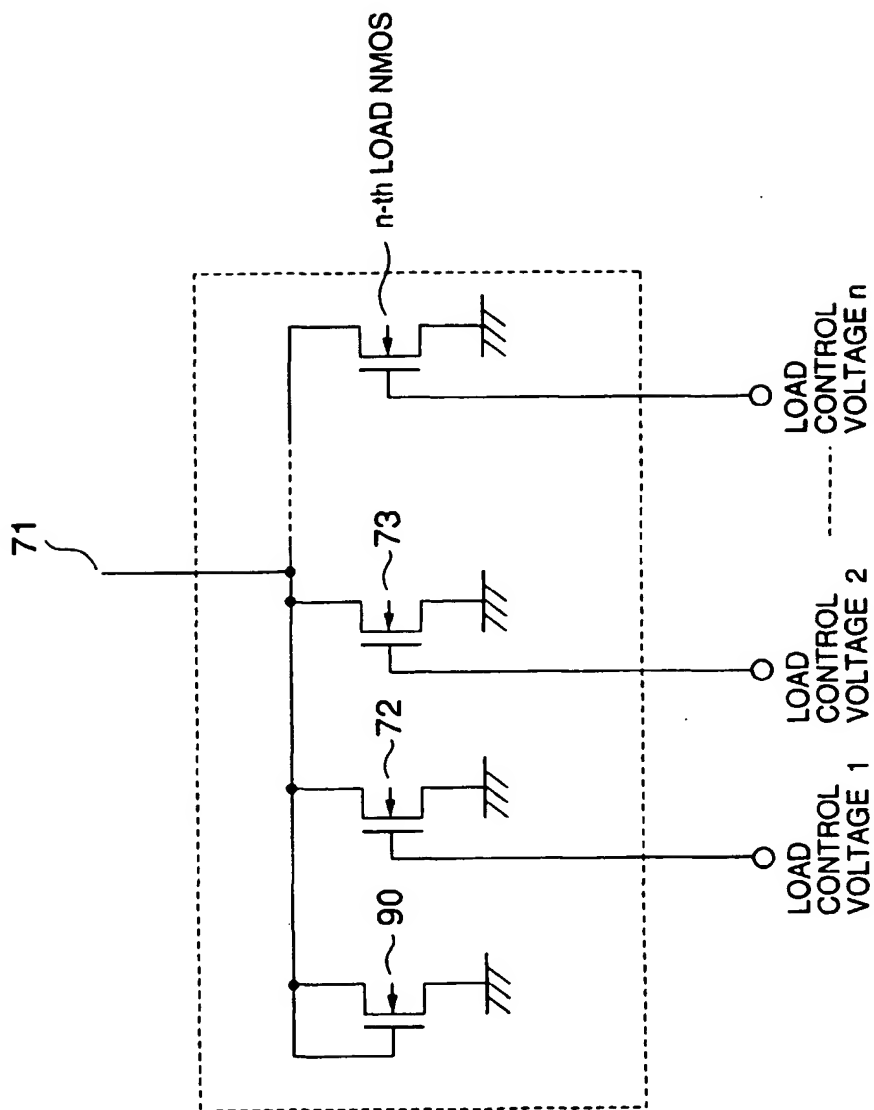


Fig.13

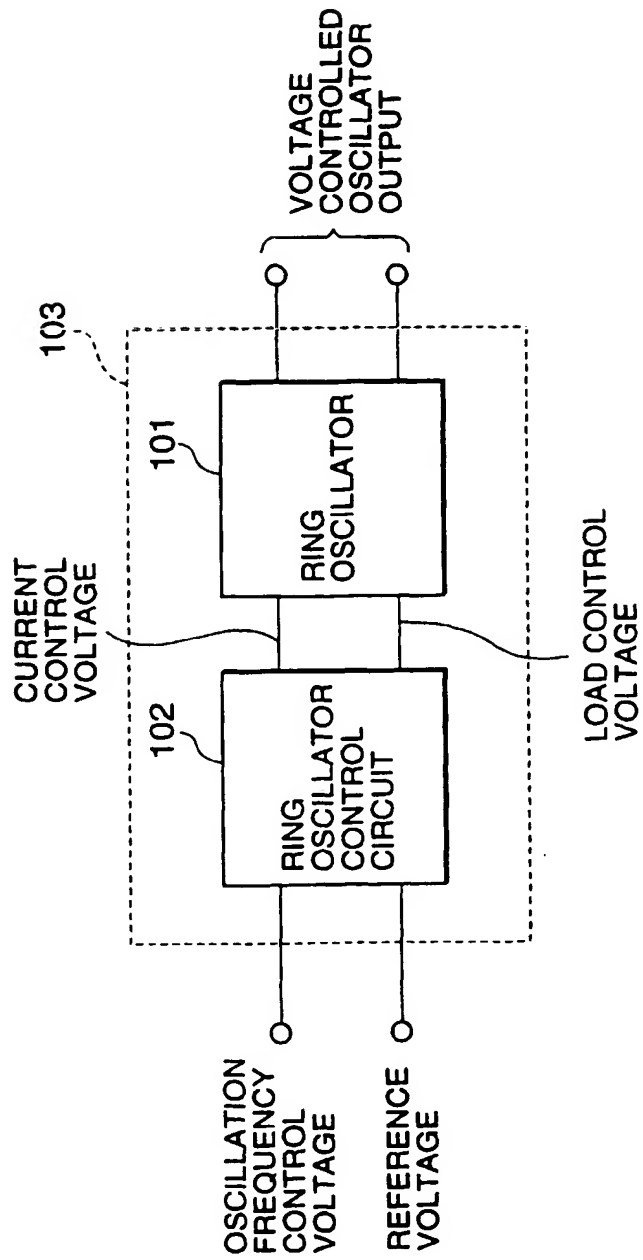


Fig.14

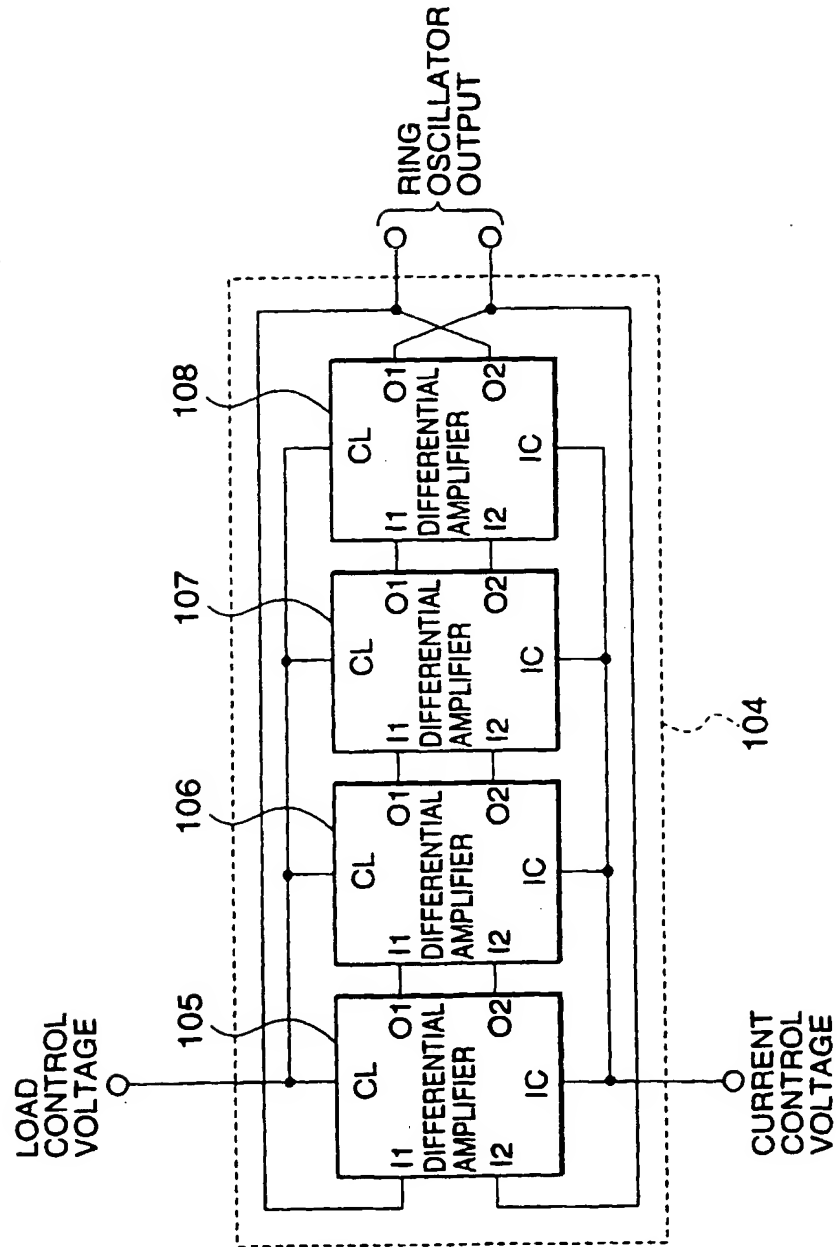


Fig.15

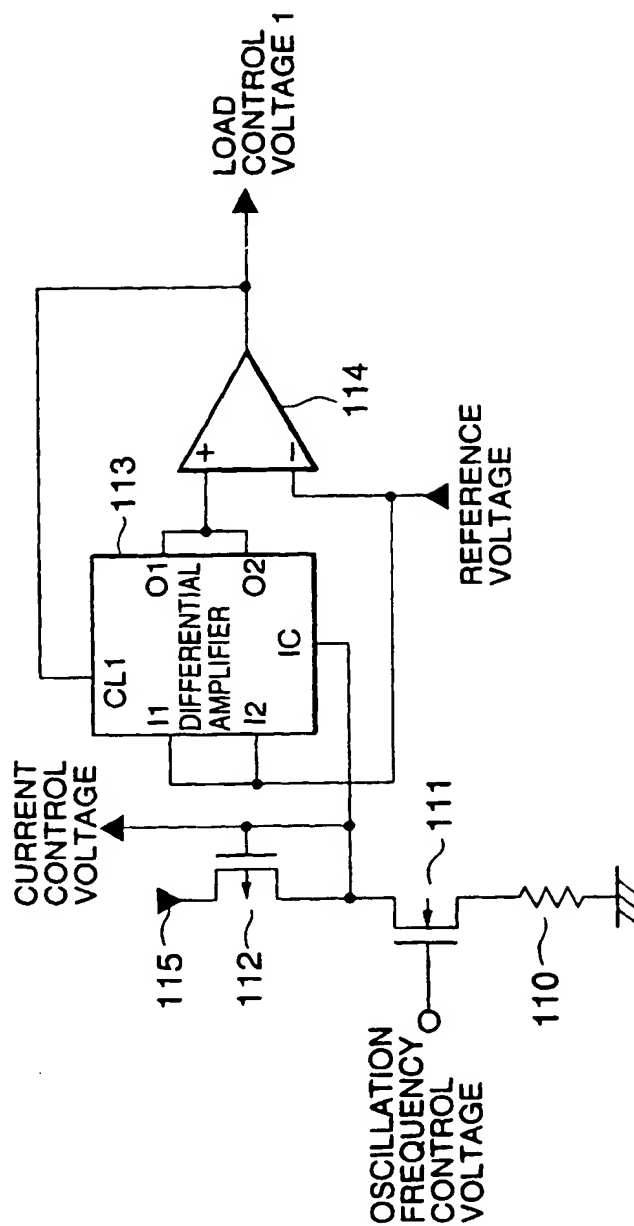


Fig.16

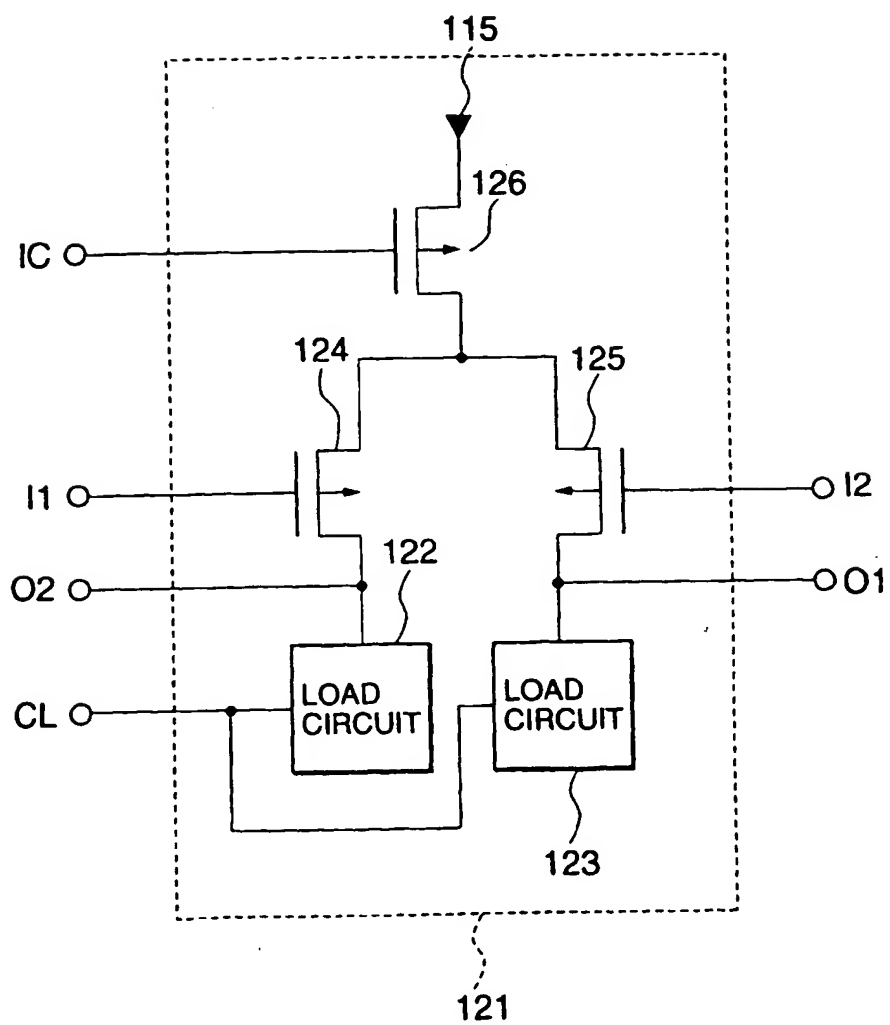


Fig.17

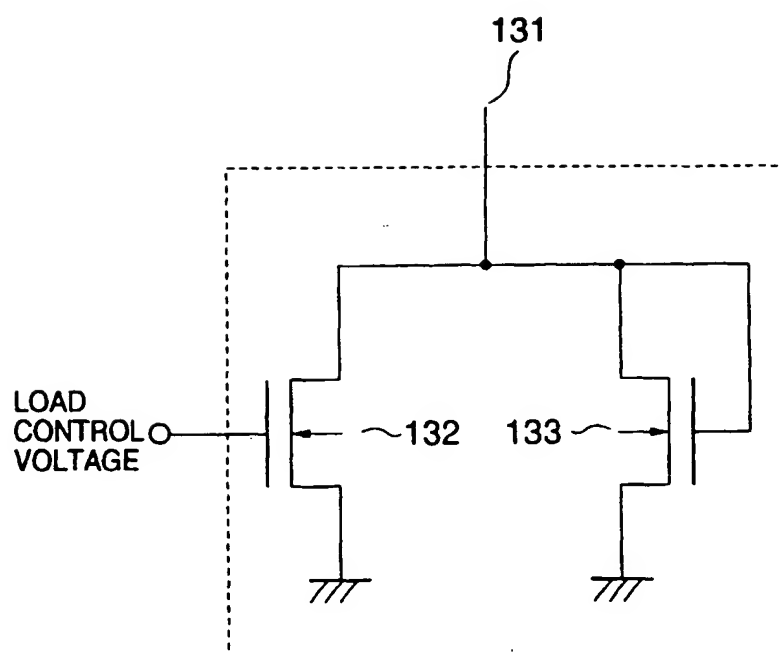
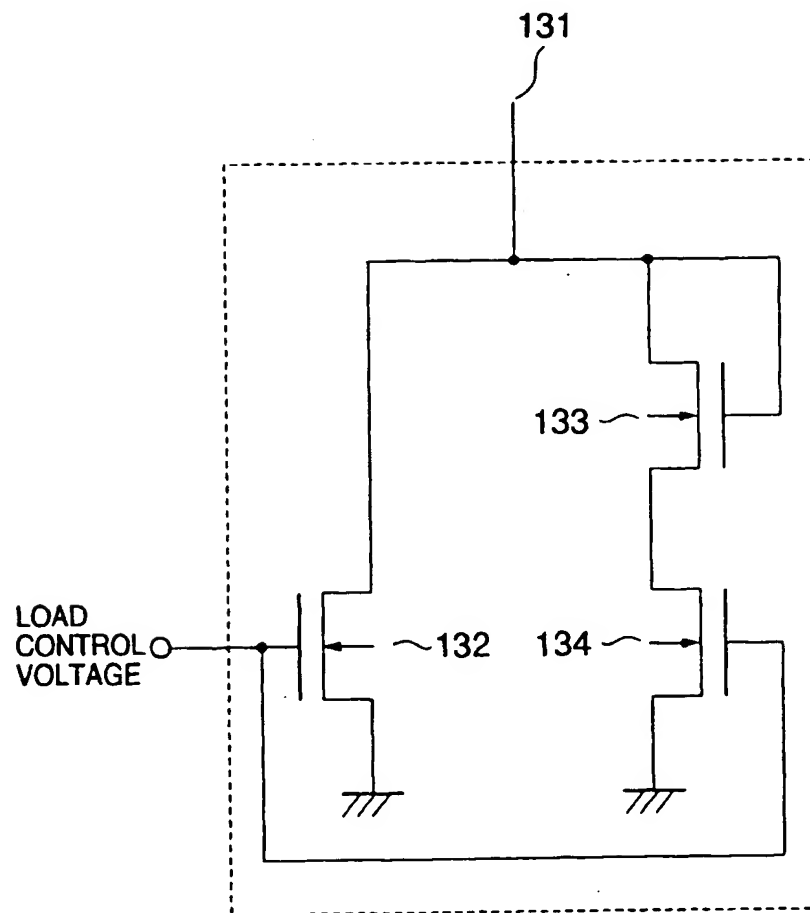


Fig.18





European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 00 10 9234

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 821 823 A (BEREZA WILLIAM) 13 October 1998 (1998-10-13) * column 5, line 43 - column 5, line 55 *	1-3,8	H03L7/099 H03K3/0231 H03B5/24
X	US 5 264 785 A (GREASON JEFFREY K) 23 November 1993 (1993-11-23) * column 3, line 60 - column 4, line 58 *	1-3	
A	US 5 563 553 A (JACKSON HARRY S) 8 October 1996 (1996-10-08) * column 4, line 4 - column 5, line 7 *		
A	US 5 515 012 A (BHUSHAN BHARAT ET AL) 7 May 1996 (1996-05-07) * column 5, line 8 - column 6, line 51 *		
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
			H03L H03K H03B
The present search report has been drawn up for all claims			
Place of search MUNICH		Date of completion of the search 26 July 2000	Examiner Kahn, K-D
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ON EUROPEAN PATENT APPLICATION NO.**

EP 00 10 9234

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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26-07-2000

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 5821823	A	13-10-1998	EP	0895354 A	03-02-1999
US 5264785	A	23-11-1993	NONE		
US 5563553	A	08-10-1996	NONE		
US 5515012	A	07-05-1996	EP	0771491 A	07-05-1997
			WO	9637044 A	21-11-1996

EPO FORM P448

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82